UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,412,468 B2
APPLICATION NO. : 10/686331
DATED : August 12, 2008
INVENTOR(S) : Richard M. Butler

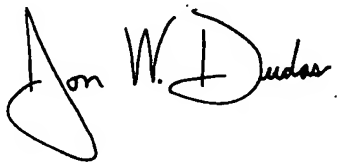
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 10, line 58, in Claim 1, delete "MISRs." and insert -- MISRs; wherein the inputs of at least one of the number of MISRs are coupled to at least one of a data address bus which transfers data addresses between a data address cache and a CPU core, an instruction data bus which transfers instructions between an instruction data cache and a CPU core, and an instruction address bus which transfers instruction addresses between an instruction address cache and a CPU core. --, therefor.

In column 12, line 27, in Claim 19, after "address" delete ":" and insert -- ; --, therefor.

Signed and Sealed this

Eleventh Day of November, 2008



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